

Op-Amp Audio

Realizing High Performance: Buffers (Part I)

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In this and the next few columns, we will take a departure from the immediate past, and focus some overdue attention on real circuits. We'll cover some op-amp issues related to realizing high performance in audio and other ac applications. This venture has been inspired in part by reading some USENET newsgroup postings, with such confidence-boosting headers as: "Op Amps always inferior to discrete?" and others equally as upbeat in tone.

While I can't promise any panaceas, I do have confidence that a greater understanding can come from some focused discussions of op-amp audio pitfalls. Topics to be covered are: buffering, the IC op amp's best friend (this and next installment); matching an op amp to an audio application; and op-amp wisdom and witchcraft.

How many inputs does an op amp have? I find it useful to look at op-amp performance in terms of errors in response to various inputs. These inputs can come via the normal differential ones at pins two and three, plus at least three others. Aha! Stumped on that one? So, what else constitutes an input, beyond the two familiar power-supply-rejection-ratio (PSRR) errors for an amp's +VS and -VS terminals, disregarding any offset pins?

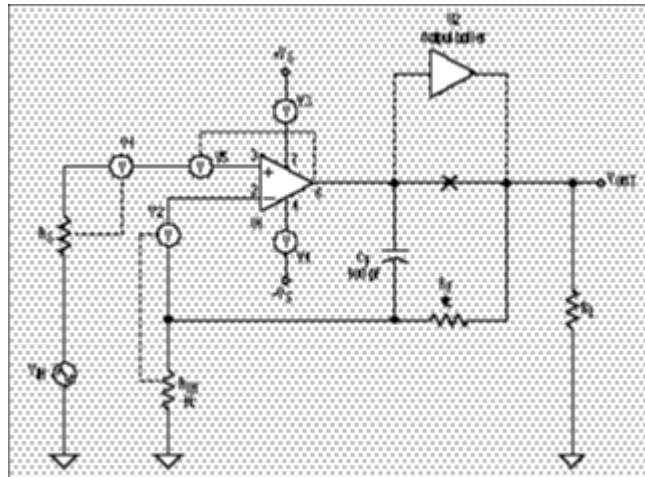
Well, it may or may not be obvious, but the output terminal of an IC op amp can actually be the source of the fifth input error, one which results in load-induced changes in offset voltage. Although all modern, single-IC op amps are designed with thermally symmetric, input-stage layouts vis-a-vis the output (for minimum thermal feedback), life isn't completely perfect here. Consider the fact that just microvolts of undesirable offset change can be significant at low audio frequencies. Take a 5-MHz bandwidth op amp as one example, where a 1-V p-p/100-Hz output swing requires an effective 20- μ V p-p differential input.

So, whatever their source, extraneous signals might easily be comparable to actual signals of this magnitude. In a low-noise, bipolar-input op amp, a thermal change resulting in a few degrees Celsius temperature differential to the input stage might induce a fraction of a microvolt or more offset shift. Although such an error seems numerically small, it's still relatively large with respect to a 20- μ V p-p, real signal. The point is not that this example represents any real device or conditions. It is more to frame some perspective and sensitivity for monolithic-IC-based technology, and the resulting application implications.

The figure shows a typical op-amp gain stage, configured here as an example application with an ideal gain of 5x, driven by a signal V_{IN} . The previously mentioned op-amp error sources are as noted, represented by sources V_1 to V_5 . The dotted lines are intended to convey a general relationship of a given error to the source.

For example, the output-power-dissipation-related errors are reflected back to the op-amp input as a

thermally coupled offset change, V5. For this installment of the overall discussion, I'll concentrate on this error, picking up the others further down the road.



Both single, as well as multiple, op amps built on common monolithic substrates can be susceptible to thermal errors. This is simply because a potentially high-dissipation output stage and the error-sensing input stage are part of the same basic monolithic IC chip. In the classic reference, thermal effects in IC op amps were discussed, and modeled as an additional feedback path, which can limit available gain.¹

It is worth noting that IC designs are a diverse extreme away from conventional pc-board discrete circuits, which are by definition, loosely-coupled thermally. Hybrid op amps may or may not be thermally sensitive, depending on their specific substrate and layout details. Modular op amps should be relatively insensitive to thermal effects, unless potted with a thermal compound.

Testing for thermal errors: Quantifying op-amp input-offset errors due to output loading isn't totally straightforward, but it isn't impossible either. For audio-oriented use, one straightforward technique is to measure output THD+N and/or other distortions under both heavy and light output-loading conditions. This will reveal degradation due to thermal-coupling effects. However, dc and low-frequency testing may actually give some greater insight into what happens to an op amp as it undergoes heavy loading. This is because one can literally see the changes in transfer function, as output loading changes.

Relatively simple, dc X-Y plots can give visual indications of amplifier linearity under load. See Reference 2 for an example of a single-op-amp test circuit for plotting amplifier input drive on the Y axis vs. loaded \pm output swing on the X axis. This test is easily expanded to include loaded and unloaded comparison conditions, which can then reveal dynamic-thermal-error components, as well as transfer nonlinearity.

For this article, I modified the test circuit as follows. I changed the summing-node attenuation resistors from $1M\Omega/10\ \Omega$ to $100\ k\Omega/10\ \Omega$, added a $10\text{-}\Omega$ balancing resistor in the positive input, and made the total load resistance $530\ \Omega$. To test various op amps, I made the offset trim universal by summing a stable, variable \pm voltage into the $10\text{-}\Omega$ summing resistor via $100\ k\Omega$. If you repeat this setup, use clean, well-balanced layout techniques and stable supplies, and you'll be able to observe $1\ \mu\text{V}/\text{division}$ on your scope.

These steps make the new VY error scaling $100\ \mu\text{V}/\text{V}$, which is easily sensitive enough to see μV -

level input changes with 10-mV/division scope scaling. The display allows you to measure loaded and unloaded gain, as well as associated changes in slope, which represents device nonlinearity.

With a ± 10 -V output, and 530- Ω loading, nonlinearity is readily evident with standard 5534 audio IC op amps. In one sample, the offset shift and slope changes from low load to full load. This results in about 60 μ V of offset change, with a steep slope change with polarity reversal (although this is a large shift in terms of the error change, it is still relatively small vis-a-vis the ± 10 -V output).

Precision low-noise op amps such as the AD797 and LT1115 are much more well-behaved for this test, with similar-conditions errors of about 1 μ V, and no radical slope changes. Look for low- and linear-slope errors, which represent linear gain, as opposed to radical changes and transfer function kinks.

Dual IC op amps are very popular, and can also be easily tested for power- dissipation-related crosstalk.³ One of the more simple, yet useful tests, is to connect channel A of a dual op amp as a grounded-input follower, with channel B configured in a closed-loop, gain-of-1000 circuit. By driving current into the A side, A-B thermal coupling can be measured at the B output. By controlling the polarity, frequency, and duty cycle of the driving current, useful information on a device's channel-to-channel thermal coupling can be obtained.

What may be surprising about some thermal errors is the relatively high frequencies at which they can be noticed. For example, a dual-output power-driver circuit, using a composite topology can be monitored for the effects of thermal crosstalk between the driven and undriven channels.⁴ Crosstalk components were noted up to several kHz.

Minimizing thermal errors: By using one or more of the tests above, various amplifiers can be exercised for thermal errors, and comparisons can be made to find types with the lowest thermal errors for loaded conditions. But, audio op amps tend to be more specialized, and it may be that your favorite chip just doesn't look so good for thermal errors. Not to worry, there is still a worthwhile system solution, one which really turns out to be optimized for solving thermal problems and maximizing performance.

As shown in the figure, the answer is to simply split the voltage amplification (U1) and power-delivery functions (U2) by buffering the output of an IC op amp with a dedicated circuit, chosen (or designed from scratch) for more-than-sufficient drive current. The burden of current delivery and associated power dissipation is simply (entirely) removed from op amp U1. This is shown conceptually as the optional (dotted connection) buffer stage in the figure. The buffer is activated by breaking the output line at "X," and connecting the unity-gain buffer U2 as noted.

With the buffer used, the main feedback path through RF is taken after the buffer, and across the load, RL. The buffer circuit proper may include some specific details, such as bypassing, parasitic suppression resistances, etc.; this will be an individual thing. There should almost always be some sort of isolation impedance between the buffer output and the output terminal, to isolate any cable capacitance. This can either be a small, 20- to 100- Ω resistor, or the LR network described in Reference 4.

There is also a high-frequency, ac-feedback path through CF, which has the effect of removing the buffer from the circuit at very high frequencies, in this case at $1/(2^{1/4}RF_{CF})$. This also aids with

stability when driving long cables or other difficult loads.

Choosing a buffer circuit: One has a basic two-path choice- an IC or a discrete circuit. ICs tend to be more desirable from points of size and efficiency, but they may not be lower in cost, or useful beyond about several hundred mA in non-heatsink packages. Discrete circuits can be tailored for any current level, but they tend to be quite busy in terms of component count, especially with such bells and whistles as current limiting and protection circuits.

Performance-wise however, both of these circuit approaches to buffering can be used, and either will allow the highest realizable performance for a given op amp. If an IC buffer is used, one can almost have the cake while eating it, too. This is done by packaging a simple, four-lead IC buffer like the BUF04, and a highly linear IC op amp such as the AD744, together as a (isolated) two-chip solution in a common package. Other dedicated IC buffers I have used successfully in the past have been the OPA633, EL2003, LT1010, LH0002, and LH0033, all of which deliver ± 100 mA (or more). Video op amps like the AD811 and AD817, also work well as buffers, due to their good linearity and high-current output stages.

The U1 op-amp-circuit part can really be left to optimize from other standpoints. Whatever it is, it will be most happy when lightly loaded via a fast, linear, high-current buffer.

TIP: In the next installment we'll look at some more issues associated with buffering, and describe in detail a suitable discrete-circuit version.

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Solomon, J., "The Monolithic Op Amp: A Tutorial Study," IEEE Journal of Solid State Circuits, December 1974; Vol. SC-9, No. 6.

"Open-Loop Gain Linearity Test Circuit," Figure 3, Analog Devices OP177 data sheet.

"Crosstalk from Thermal Effects of Power Dissipation," Figures 24-26, Analog Devices AD708 data sheet.

Jung, W., "Composite Line Driver with Low Distortion," Electronic Design Analog Applications, June 24, 1996, p. 78.

Op-Amp Audio

Realizing High Performance: Buffers (Part II)

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Taking up where last month's column left off, here's the second part of our discussion on output-buffer techniques as part of audio op-amp applications.

A flexible Class A buffer: To fulfill the function of the discrete version of a unity-gain buffer, consider the schematic in the figure. A number of features lend this circuit utility, and can either be built as-is or modified for specific needs. Functionally speaking, this buffer's intended to drop directly into the U2 stage of last month's general diagram.

The hookup's basic function is that of a complementary buffer, with a nominal input/output dc offset near (but not exactly at) zero. Actually, this is quite a common circuit type. It's often realized with a complementary output transistor pair, biased in turn by a pair of forward-conducting diodes driven at their midpoint by the input op amp. I used such a circuit years ago in my op amp book.¹

Here, replacing the two diodes with complementary transistors still has the same basic advantage of near-zero input/output offset. But, it lowers input bias current substantially, due to the transistor gain. It can also reduce distortion due to better load isolation.

The cancellation of the forward VBEs of Q1-Q3 and Q2-Q4 is somewhat imperfect, however, as these are different device pairs. Output transistors Q3 and Q4 are 1-A types, for best gain linearity at 100 mA or more current peaks. Driver-stage devices Q1-Q2 are general-purpose types, suitable for currents of up to 100 mA and more (much higher than used here). A version of this general complementary topology was used in the classic LH0002 buffer, where the Q1-Q2 emitter currents were set simply by resistors to the supplies. A discrete version, the "0002," was also offered.²

In this case, the respective Q1-Q2 emitter currents are set up by current sources, Q5 and Q6. Their output current levels, along with the use of emitter-stabilization resistors R3-R4, work to indirectly set up the output-stage quiescent current. With about 4.5 mA of current flowing in R3, Q1 is biased stably. With the VBEs of Q1-Q3 nominally equal, it can be seen that R3 and R6 will drop comparable voltages. This means that Q3 will conduct about twice the current in Q1, for the 2:1 ratio values. Thus currents set by Q5 and Q6, along with the relative resistance ratios, determine the output quiescent current.

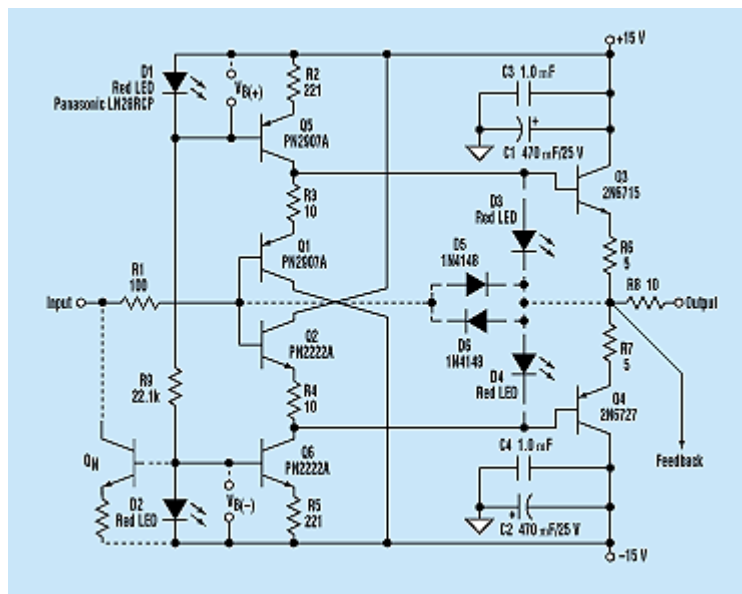
Here, the VBEs aren't exactly equal between complements Q1-Q2, or for Q1-Q3, and the idle current in Q3 is more than 10 mA (about 13 mA). Similar reasoning applies to Q2-Q4. Either more or less output-stage current through Q3-Q4 can easily be affected, simply by adjusting the relative values of R3/R6 and R4/R7 together. This is best done via the choice of R3-R4 value, leaving R6-R7 fixed.

At 13 mA of current in Q3-Q4, they operate rather rich in Class A mode—at least until heavier loads

should appear. For this bias level, departure from Class A will occur somewhere around 1.5 V, for a 150 Ω load.

The Q3-Q4 dissipation is about 200 mW each on ±15-V supplies, which will be OK for plastic-packaged devices like the original TO-237 devices, or the Zetex "E-line" version. Either of these packages should be used with ample pc-board copper area on the collector leads to aid in heat transfer. All circuit parts are available from international suppliers, such as Digi-Key.3

If much higher sustained currents are needed, even lower-thermal-resistance device packages can be used with Q3-Q4, such as the MJE171/181 or D44/D45 families. And, a lower-output-current version can be implemented by using PN2222A and PN2907A types for Q3-Q4.



Protection of this circuit is provided by several means. Without D3 and D4, the upper current limit for Q3-Q4 is set either by the limited-drive current (5 mA) times the gain (50 to 250), or by the R6-R8 values and the supplies. This current can easily reach several hundred mA, so active current limiting is very useful. The optional Red LEDs D3 (D4) provide this, clamping the drive to Q3 (Q4) when the emitter current reaches about $1.2/R6$, or ~240 mA as shown. For lower levels, the LEDs don't conduct and signals pass normally. The LEDs are Panasonic types as noted.

When used within an overall feedback loop with an op-amp driver feeding R1, this buffer might need protection from overvoltage. The optional diode clamps D5-D6 provide this function. They clamp the drive to Q1-Q2 when and if the R8 output is shorted- so large reverse voltages aren't seen in the circuit. With normal signals, there's just a few mV across the diodes and they don't conduct.

Performance: Ideally, a buffer such as this is transparent to signals with differing loads and with diverse levels. The circuit shown was tested standalone-that is, with no driving op amp. Tested for THD+N with both low- (150 Ω) and high-impedance (100 kΩ) loads, it holds up well over levels from 0.5 to 8 V rms. At the highest levels of 8 V into a low impedance, THD+N reaches a high of 0.15%. But, it quickly drops to 0.02% at 2V, and is appreciably less than .01% at 0.5 to 1 V, or within the Class A range.

For high-impedance loading, distortion for all levels is well below 0.01%, typically 0.002% for 1 V. And, for either load impedance, THD+N is also relatively independent of frequency (below 100

kHz). Harmonics within the distortion residual at the output are predominantly third at 1- to 2-V levels.

The circuit's output impedance is essentially resistive and about 15 Ω , most of which is the R8 value. Voltage offset of the buffer will be high, in the 20- to 30-mV range, due to the inexact VBE cancellations. When used within an overall feedback loop, as illustrated last month, this offset isn't consequential. It's suppressed by the feedback loop.

Housekeeping details: Some parts of the schematic aren't directly involved with the buffer function, but nevertheless still have utility. An example is the optional npn current-source transistor, QN. This can be used to set up a fixed-current drain directly from the driving op amp's output stage, thus operating it in a richer-than-normal Class A current range and minimizing any internal Class AB effects for alternating output-signal polarities. By using the high dynamic impedance of a transistor for this function, a fixed steady current can be taken from the op amp without loading it dynamically (and possibly increasing distortion). QN's LED bias scheme of $V_B(-)$ will cause a current of 1.2 V divided by the emitter resistance to flow in the collector. For example, 1 k Ω would source 1.2 mA. For opposite polarity (current sink) loading, a pnp current source "QP" is biased by D1, with a similar emitter resistance. If used, QN or QP are PN2222A or PN2907A types.

As noted, this buffer circuit functionally drops into the hookup of last month—that is, between the op amp and the load. The feedback path is taken before isolation resistor R8, providing simple, effective load isolation for the buffered op amp.

When driving low-impedance loads, decoupling of the high-load currents is accomplished with large, local electrolytic bypasses C1-C2, with their shared point returned to the load common. Because of the wide transistor bandwidths used, layout and wiring can also be critical. C1-C2 should be augmented by local, low-inductance high-frequency bypasses, such as 1- μ F/50-V stacked-film types C3-C4, located physically near Q3-Q4.

It's worth noting that long lines, which appear as a capacitive load, are low-impedance loads. Even if terminated at the far end in a moderate resistance value (\sim 10 k Ω)-for high frequencies, the effective load such lines present to the amplifier is still low (XC for 10 nF looks like 800 Ω at 20 kHz). R8 is a load isolator, and can be increased if necessary.

Further suggestions: It should be obvious that this circuit is readily adaptable for various needs. If used on other supply voltages, the current in LEDs D1-D2 would benefit by being stabilized, perhaps by something as simple as a 1-mA JFET current diode in place of R9.

The output transistors (and their operating point) are best chosen to maintain the lowest distortion for the particular loads and operating level. Remember: The distortion figures quoted are for the buffer alone. A well-chosen driver can lower it even further.

TIP: These first two installments on high-performance audio with ICs and discretely have focused on choosing (or designing) a buffer stage for best overall performance. In IC op amps with poor thermal design, heavy output loading can cause shifts in effective input offset, as well as associated linearity changes. These load-dependent shifts can be identified with testing, allowing easier device selection to minimize this problem.

However, simply buffering the amplifier's output with an isolated-package circuit removes this source of error, and maximizes op-amp linearity. This step is recommended wherever it's practical

and needed. Buffer circuits can be chosen from a number of ICs expressly designed for such tasks, as was noted last month. Or, they can be designed to match a given set of conditions, as in this example.

The ability to adapt and hone a circuit's operational characteristics precisely to an application is a major hallmark of discrete circuitry, as this example shows. In contrast, adaptability to different drive and bias levels isn't something IC buffers can do, at least not in the manner here. One needs to choose either the flexibility and diversity of the discrete approach (at the expense of component count), or the small size and component efficiency of the IC approach (at some expense of bias and drive flexibility). In any event, enjoy those low distortion, Class A sounds!

Acknowledgments

In preparing the last two columns, I appreciated helpful comments from audiophile friend and design consultant John Curl.

References

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Digi-Key Corp., 701 Brooks Ave. South, Thief River Falls, MN 56701-0677; (800) 344-4539; <http://www.digikey.com>.

Op-Amp Audio

Realizing High Performance: Bandwidth Limitations

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For this November Analog Special installment, we'll take a look at some of the very basic issues surrounding op amps used within high-quality audio circuits. A parameter which ultimately affects a gamut of op-amp performance specs is device gain-bandwidth. This is related to the device's open-loop bandwidth and gain in predictable ways. These interrelated issues, along with the nature of the feedback for a particular application, ultimately become major quality determinants.

The open-loop bandwidth problem: Virtually all conventional voltage-feedback-type op amps have a high open-loop gain (* 100 dB), and a relatively low open-loop bandwidth (10 to 100 Hz). By voltage feedback, we specifically mean the classic op-amp types with symmetrical \pm inputs, and are excluding current-feedback types (at least for now). Of course, this voltage-feedback category includes audio-specialized types, as well as more conventional non-audio ones.

All such amplifiers are designed to be flexible and easily applied within an overall feedback system with closed-loop stability usually down to unity gain. For unity-gain stability, the application of feedback demands a controlled rate of open-loop roll-off. This roll-off is a uniform 6 dB/octave gain reduction with frequency. The associated 90° phase lag of such an open-loop response will guarantee closed-loop stability for any feedback level.

But herein lies the rub. What seems like a relatively simple system trade-off in design philosophy may not actually be so. Why is this? Isn't any op-amp-based audio design more simple than a classic RC-coupled transistor gain stage? A more complete answer here is a rather complex one, and it involves an understanding of the feedback process. It also involves implications of applying the feedback around what can often be imperfect amplifier hardware. For example, a nonlinear op-amp input stage, combined with less-than-optimum-bandwidth.

We do know that an op-amp-based gain stage can be just about as simple as it gets system-wise-at least on the surface. It consists simply of the op-amp device itself, plus a pair of resistors to set the desired gain (see the figure from Part 1, Electronic Design, Sept. 1, p. 166). Unfortunately, the underlying weaknesses of how such a feedback-based amplifier can degrade some aspects of overall performance often gets bypassed, particularly when there is pressure to employ only standard, low-cost ICs (such as 5532 types and their derivatives).

An op-amp gain stage is unrivaled in utility, a feature which is very compelling. But, it trades off open-loop gain for bandwidth, operating within the constraints of a constant gain-bandwidth product. For the 5532 mentioned, the applicable gain-bandwidth is 10 MHz, and the open-loop gain is 100 dB (105 V/V). Thus, the open-loop bandwidth is 100 Hz. Actually, a close examination of the 5532 data sheet shows more like 200 Hz, due to the fact that this particular topology uses a feedforward technique, which boosts gain-bandwidth at lower frequencies. But, in general, the available small-signal gain at any given frequency is defined by the op amp's gain-bandwidth. Note

the emphasis here on the small-signal aspect. And, it's helpful to understand that the application of different feedback does not change a given device's basic gain-bandwidth-it only reallocates it to some different closed-loop gain and bandwidth.

All of this may seem reasonable enough, until we go a step further, and consider the fact that the op-amp gain-bandwidth is based upon the small-signal transconductance (g_m) of the input-stage transistors, plus a fixed compensation capacitor (usually internal). If we consider this compensation cap fixed (for this discussion, at least), it should be obvious that the g_m of the input devices is also fixed, ideally. In other words, it doesn't vary with the input signal level.

But, within real devices, the g_m most certainly does vary. In fact, those devices that are best in terms of voltage noise performance-bipolar junction transistors (BJTs)-are worst in terms of their transconductance linearity. Barrie Gilbert has explored many of these non-ideal op-amp performance limitations in some recent EDTN columns.^{1,2} Reference 2 includes a mathematical distortion analysis of an op amp. The analysis shows how an undegenerated BJT input stage (as just described) is actually quite poor in terms of standalone-mode distortion. The fundamental source of this distortion is the nonlinear g_m of the emitter-coupled BJT pair, which follows a hyperbolic tangent (\tanh) function. Ideally this g_m would be highly linear, i.e., the inverse of a fixed resistance. While it isn't linear with a simple emitter-coupled BJT pair, it's much more so when the pair is operated with emitter-degeneration resistors, or the bipolars are replaced by JFET devices.

In an op-amp feedback circuit using such a nonlinear BJT input stage, the forward gain path typically includes the input stage as described, followed by an integrator stage which includes the aforementioned compensation cap, and a final output stage for load isolation.

When such an amplifier is placed within a simple, flat-frequency-response feedback setup, it's useful to contemplate what happens with a wideband audio signal passing through it. Consider, for example, a given input-signal level, and a flat voltage vs. frequency characteristic at the output. Increasing signal frequencies above the amplifier's open-loop corner frequency will result in a higher and higher input driving voltage to the op amp. (Not the signal input, but the actual voltage between the \pm terminals.) This is a natural consequence of the feedback error correction, and the gain-vs.-frequency reduction within the op amp.

But, since the BJT input stage g_m is nonlinear, and is followed by a low-pass filter in the form of the integrator, higher signal frequencies require higher amplifier driving voltages to maintain the same output levels. This means higher frequencies must necessarily drive the input stage harder, to counteract the filter roll-off. Because the input stage's g_m is different with a greater input drive, it produces a different corner frequency and phase shift (compared to lower frequencies, which require less amplitude drive). Considering just a case of one output level, this is a frequency-dependent nonlinear phase response.

When the output level is further increased, this phenomenon gets worse, until at some combination of amplitude and frequency, the op amp finally reaches its slew-rate limit. By definition, this occurs when the input stage is totally overloaded by the peak error voltage, at which point the output voltage from the op amp reaches its maximum rate-of-change.

So, in the absence of any corrective means, it can be shown that virtually all BJT-input-stage op amps (either IC or otherwise) can be limited in terms of input-overload sensitivity. And, they are nonlinear prior to their overload point. This is due to their extremely high and exponentially related

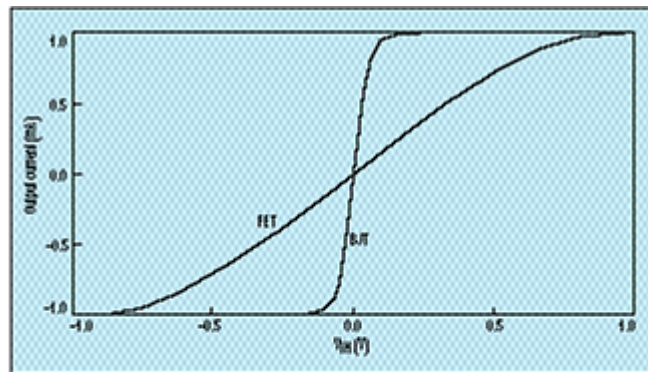
gm.

To put all of this in an overall perspective, a balanced BJT differential pair will develop around 1% THD for input signals which are just under 20 mV in peak amplitude. When such an input stage is used within a 10-MHz-gain-bandwidth op amp handling a 20-kHz, 10-V peak output signal, the actual amplifier driving signal will be 20 mV peak-it is just beginning to distort. If the amplifier were instead a 1-MHz "741-speed" device, the driving signal theoretically would be 200 mV peak. In practice, such an amplifier would more likely be operating in its slew-limited mode, and producing gross output distortion.

For today's audio op amps with bandwidths of 10 MHz or more, it could be argued that only the most extreme high-level, high-frequency audio signals even begin to push a non-degenerated BJT-input op amp into the nonlinear region. On the other hand, for digital signal byproducts, and other spurious out-of-band high-frequency components, the distinction may not be so clear. Here, an amplifier with more-linear input stages may be a better choice. And, if you've ever experienced spurious AM-band signal detection by a bipolar input stage op amp, you'll be able to relate to all of this, for sure!

A positive aspect of this situation is that the BJT-input amplifier can easily achieve low input-noise performance, and it is good for low-level signals. But, the not-so-good side is that it can possibly show increasing distortion and phase shift effects for high-level, high-frequency signals above the open-loop corner frequency.

Comparing BJT/JFET gm: Since op-amps are available with front ends consisting of either bipolar or JFET transistors, it is useful to compare them for overload. The gm characteristics of both 2N2222A npn BJT and 2N5457 N-channel JFET differential-pair transistors make for a good comparison (see the figure).



The relative transconductance characteristics for a ± 1 -V input range are displayed for both BJT and JFET differentially paired transistors. Both types use no emitter (source) resistance, and are biased by a fixed current of 1 mA. These curves were generated by PSpice, using 2N2222A and 2N5457 models available with that simulation package.

In these simulation plots, both transistor pairs are biased at the emitters (sources) by a 1-mA current source. The BJT-pair output is represented by the more steeply sloped trace in the center, with an

input dynamic range of about ± 200 mV for the ± 1 -mA output current. Also shown is the more-linear, gradually sloped gm plot of the JFET pair, which has an input dynamic range of nearly ± 1 V for the same output current. That is quite a contrast!

These data indicate the two major points just discussed above. Namely, that the BJT-device gm is both higher and more nonlinear than that of the JFET. In fact, the degree of nonlinearity for the BJT case isn't readily apparent from this view, but it is easily revealed by comparing plots of differentiated data.

Extending open-loop bandwidth: Since the presence of an amplifier open-loop corner within the audio range, combined with feedback around a nonlinear BJT input stage, can give rise to dynamic phase shifts, a question arises: what can be done counteract it? Solutions are available in 3 forms.

1. One solution is by extending the effective open-loop bandwidth, so as to move the open-loop corner upward to 20 kHz or more. This step doesn't change the distortion in the input stage. But, it can reduce or remove the phase-modulation effects due to gm variations-as the open-loop corner is moved upward to a region where (presumably) signals either do not occur, or they occur less frequently, or at lower levels.

The route to achieving this step can be as simple as adding one (or two) resistor(s) across the amplifier integrator. This damps the integrator and lowers the open-loop gain, thus moving the open-loop corner upward in frequency (again, within the constraints of the device's gain-bandwidth product). Practically, this step is not available on many amplifiers, but those with single-node comp pins and a zero-dc-offset output stage will allow a single such resistor to be added. One example is the AD829, with a compensation pin at pin 5, and a low-noise BJT input stage. Other amplifiers may require two resistors, one from the output back to one of the null terminals, the other from the opposite null terminal to common. For example, the 5534 can be used in this fashion with nominally equal value resistors from the two null pins. A significant trade-off of this approach is that the device's dc offset will almost surely be compromised by this inner-loop connection. This can in theory be corrected by a trim adjustment, but this step isn't likely to be practical.

Unfortunately, there are no common standards of what pin(s) are used for these secondary-bandwidth control functions, or what the relevant resistance(s) are, so some user experimentation is appropriate here, once given the proper amp.

Viewed from a system-level perspective, there's a more elegant and less compromising solution to optimizing the open-loop bandwidth of an op-amp circuit. Use multiple-stage feedback, so that the overall input- stage-to-integrator interface is controlled by local, signal-independent transfer characteristics.

Of course, this is a much more complex solution, and a useful working example will need to wait until a later installment. It also happens to be about the only practical way one can realistically implement the open-loop bandwidth control trick using dual (or quad) amplifier packages.

2. Use more-linear devices for the input transistors, which lessens the signal phase-modulation problem by reducing gm nonlinearity. This is simply achieved by using a well chosen-op-amp. For example, one using a JFET input stage, either PFET or NFET. Both types typically have the desired lower gm. A wide variety of general purpose FET input devices are available for this task, from the TL07X series of early JFET designs, to more recent devices such as the AD744 family, and the

recent AD825 device. Of course, one does need to be selective here, as the JFET input stage is just one part of an overall picture, and other audio-relevant issues will also need screening.

3. A third (and truly optimum) method of controlling the open-loop bandwidth of an op-amp is to simply pick a device which has an inherently high open-loop bandwidth of (preferably) 20 kHz or more. While this is difficult indeed, it is certainly not impossible. And even a bandwidth of less than 20 kHz is more useful for desensitizing the phase shift effects than is a 100-Hz open-loop bandwidth. Examples are the just mentioned JFET input AD825, with an open-loop bandwidth of just under 10 kHz, or an AD817, with a similar bandwidth. The AD817 uses a BJT input stage with emitter degeneration, which gives it very good linearity.

On the downside, amplifiers that have lower-gm input stages will typically tend to be more noisy than will their lower-noise, non-degenerated BJT cousins. This makes them useful for higher-level signals, as opposed to low-level front end applications. It is another of those system-level trade-offs a designer must make in honing a final high-performance design.

TIP: One or more of these bandwidth-extension and/or linearization methods can be useful in practice, and they are recommended to you for further experimentation. In a future column, we'll show an example of a multiple-feedback-stage design which uses method 1 above for bandwidth extension and input linearization.

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Op-Amp Audio

Minimizing Input Errors

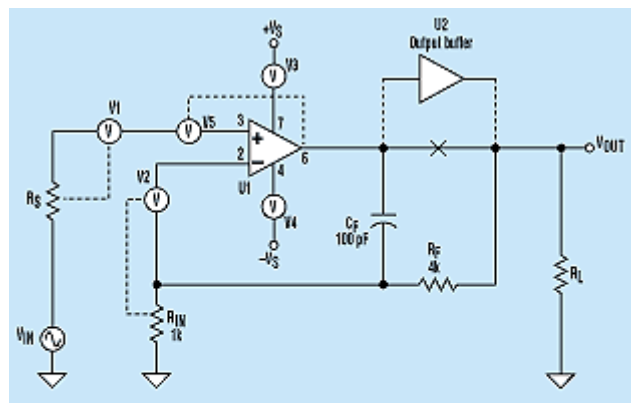
Walt Jung

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For this second December issue, the column looks at a number of op-amp issues regarding their use in high quality audio circuits. For now, this wraps up the series on this topic. As noted below, this final 1998 installment also marks my departure from this regular monthly column, in order to partake in a new project.

Op-amps and audio: Recalling the imperfect op-amp gain stage model printed in the Sept. 1 column, we will first review it with regard to the error sources, V1-V5 (Fig. 1). There is an errata note for the OP177 data sheet circuit originally referenced. It was Figure 3 on early revisions, but Figure 24 now.



1. Depicted here is a noninverting op-amp gain stage with five error sources, V1-V5. Output buffering or a load-immune op amp minimizes V5. V1-V2 are minimized by matching source impedances, and V3-V4 are minimized by careful power-supply design.

In the first two parts of the series, we discussed using buffers (both IC and discrete), along with their role in minimizing output-to-input power-related errors. This error source is symbolized by V5, with the dotted coupling indicated. With the use of an appropriate U2 buffer or load-immune op amp U1, we'll consider V5 errors negligible, and then move on to the others.

The remaining errors are V1-V2 and V3-V4, four in all. But note that these are paired error sources, so if you understand how to deal with one of the pair, you also can deal with its twin. In essence, these pairs reduce to two basic types of error sources, each with distinct minimization solutions.

V1-V2 source-impedance-related errors: V1 and V2 are ac errors, and they are proportional to the impedances seen at the op amp's (+) and (-) inputs (again as indicated by the dotted coupling). Understanding a very basic semiconductor distortion mechanism is helpful here.

A byproduct of semiconductor manufacture is the fact that often, the junction capacitance is a nonlinear function of applied voltage. Applied ac (audio) modulates this capacitance, which gives rise to even-order harmonic distortion. You can see the basis of this by studying various transistor data sheet C/V curves. Note that it doesn't matter if such junctions are within a discrete transistor or an IC, the result is the same.

For audio circuits, taking various steps can help to minimize distortion due to this nonlinear capacitance. One is to bias the capacitance to a high dc voltage. Another is keeping the ac signal swings small. A third step is to choose devices with less raw capacitance (and therefore, less sensitivity), and, finally, operating with low source impedances.

In op-amp circuit configurations, it is important to note this input stage distortion mechanism applies to non-inverting-mode operation, such as in Figure 1, where the applied common-mode (CM) voltage is highest. And, in terms of susceptible device categories, by and large it is found in op amps using junction-isolated FETs (JFETs). Note also that it is not a factor in inverting mode circuits, since by nature these don't see CM voltage.

Within JFET-input op-amps there are actually two such capacitors present, corresponding to V_1 and V_2 errors. They are directly in the signal path, with one appearing at each input terminal, i.e., the gate of the FET input devices. The capacitance is formed as part of the manufacturing process. It electrically appears between the corresponding input and one supply rail, or ac common (for p-channel FET amplifiers the rail is typically $-V_S$).

In Figure 1, source resistance R_S and the internal nonlinear capacitance of U_1 form a low pass filter at some high frequency—usually well above the audio bandwidth. However, this seemingly innocuous relationship doesn't fully reveal what can happen in sensitive, low-distortion circuits, or if R_S is high. Or, worse yet, when the op amp has appreciably higher input capacitance (as it might in the case of large-junction, low-noise input transistors). All these factors exacerbate the distortion generation.

Normally it is an audio rule-of-thumb to use low feedback resistances to minimize noise contribution. In Figure 1, the feedback source resistance ($R_{S(-)} = R_F \parallel R_{IN}$) is $<1 \text{ k}\Omega$, but the input R_S may be higher, so the amplifier's $R_{S(+)}$ and $R_{S(-)}$ aren't necessarily equal. In practice, given the very-low-distortion capability of today's op amps, (THD+N of -100 dB or better), it is easily possible to see distortion effects due to mismatched $R_{S(+)}$.

Fortunately a neat distortion solution is at hand, involving profitable use of the op amp's basic nature. Any such op amp always has two similar nonlinear capacitances, and with the input devices matched, it can be assumed the capacitors are the same. So, the distortion effects can be balanced and nulled, if within the external circuit, $R_{S(-)}$ is made equal to $R_{S(+)}$. Or, more precisely, when the total impedance seen looking out of the $(-)$ input is made equal to that at the $(+)$ input.

With an equal source impedance condition, the two sets of distortion components generated by the nonlinear capacitances match, or $V_1 = V_2$. Since this distortion is CM to the op amp (not differential), it is rejected. A distinct operational "sweet spot" occurs, with even-order output THD going to a minimum.

Therefore, to optimize noninverting op-amp circuits against V_1 - V_2 errors, choose R_{IN} and R_F so their Thevenin equivalent value is equal to R_S , which minimizes distortion. C_F , if used, can upset

exact high-frequency balance. For such cases, a compensating value can be used, from pin 3 to ground.

Wondering about your favorite op amp's susceptibility to this distortion? A good test for it is a noninverting gain stage of $2X$ (with $RS(-) < 1\text{ k}\Omega$), and RS switchable between $<RS(-)$, $=RS(-)$, and $>RS(-)$. With $V1$ - $V2$ errors, $THD+N$ plots vs. RS can reveal higher distortion for mismatches.¹

Extrapolating JFET-input op amps to even more sensitive topologies leads us to Sallen-Key active filters, which, by definition, use noninverting amplifiers (often unity-gain, JFET-based followers). For absolutely lowest distortion here, a mirror-image network " $ZS(-)$ " can be used in the feedback path, in lieu of a direct connection. $ZS(-)$ is simply a dummy RC component set, to mimic the real $ZS(+)$ filter elements, as seen looking out from the op amp's (+) input.² Other JFET-input op-amp circuits also can optimize RS , as described below.

$V3$ - $V4$ power-supply-related errors: The two remaining errors are $V3$ - $V4$, which relate $+Vs$ and $-Vs$ supply-rail noise to the amplifier inputs. These power supply rejection (PSR) errors are usually given in dB. Some might think these errors straightforward. But in real life, things are a bit more complex. Let's see why.

If you study a typical op-amp data sheet, you'll notice that there is a PSR spec for both $+VS$ and $-VS$, as well as one for common-mode rejection (CMR). But, close inspection reveals that these are dc specs. Over audio frequencies, typical PSR behavior is plotted, and it degrades with frequency at 6 dB/octave. Common values are 100 dB or more of dc PSR (or CMR), dropping to 80 dB at 1 kHz. Ironically, such popular audio op amps as the 5532 and 5534 don't provide their users PSR and CMR curves!

Also, note that PSR will often be poorer for one of the supplies, sometimes noticeably so. CMR and PSR are related—both measuring front-end response to signals common to the normal inputs, or via the rail(s) as a signal source. It is typical to specify PSR for symmetrically varying (\pm) supply voltages. Unfortunately, real-world power sources don't always vary neatly. So, a realistic audio consideration would be to analyze things in terms of the worst PSR/CMR curve from the data sheet, and use that data at various frequencies. We'll assume an 80 dB/1 kHz PSR error in an example calculation.

An error 80dB down may sound good, until we add some mitigating factors. In Figure 1, for example, the $5X$ noise gain makes an 80 dB/1 kHz error about 14 dB worse, or 66 dB/1 kHz, as referred to the output. And in almost every case with conventional op amps, this still gets worse by 6 dB/octave with increasing frequency.

Putting it in perspective with an actual output signal, we'll talk in terms of op-amp input-referred errors (since that's where PSR errors couple). Assume 1 V p-p output at 1 kHz, and an op amp gain-bandwidth of 10 MHz. This means that to produce the 1 V p-p, the amplifier's input signal will be 100 μV p-p. If the supply rail sees a 1 mV p-p/1 kHz noise (for whatever reason), this noise referred at the amplifier input will be 0.1 μV p-p. The ratio of the desired signal to the noise is 60 dB—not such a good ratio. Also, consider the possibility that CMR or PSR could be worse than 80 dB, or the power-rail noise higher.

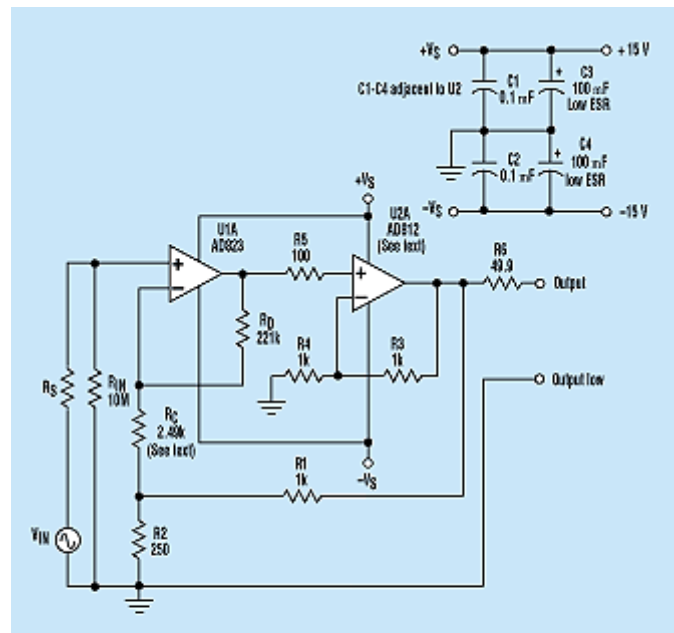
Another subtle point is that the PSR frequency-response corners for the $+VS$ / $-VS$ rails may vary from one another, and may also vary with respect to the open-loop-gain corner. Thus, the sample

numbers used here could be different in reality.

The example assumed a 10-MHz gain-bandwidth op amp. But, if we consider an op-amp with ten times the gain-bandwidth (100 MHz), the input signal reduces ten-fold, to 10 μV p-p. With the same power-rail noise, this tends towards an effect of PSR errors of similar order (80 dB) being much more serious. In practice, such a higher gain-bandwidth op-amp will very likely also have greater PSR.

The main general point being made is that real-world PSR and CMR errors can be much worse than a casual glance at a data-sheet curve may suggest. In fact, a better way to look at the topic of V3-V4 errors is to consider the rails of an op-amp simply as another signal input, and proceed accordingly. Good supply regulation and bypassing will go a long way toward minimizing and controlling these errors. In fact, it isn't unrealistic to set V3-V4 error goals referred to a working op-amp input signal of -100 dB (or better). This will generally require some careful supply regulation, since you can't always count on an op-amp providing 100 dB of V3-V4 error isolation over the applicable frequency range. Current-feedback types, for example, have typical PSR and CMR of 60-70 dB.

An optimized amplifier example: To illustrate all of the error-minimization and bandwidth-extension principles discussed in this series, the circuit of Figure 2 is offered. It can be recognized as a cousin to a previous 0.5-A line-driver/headphone amplifier.³ It also has similar thermal-distortion suppression, as the U1 stage servos out U2 thermal errors. Three distinct feedback paths are used.



2. This example design applies all the concepts of the audio series, in an optimized gain-of-five stage. In addition to minimizing V1-V5 errors, it also eliminates thermal distortion and crosstalk in output stage U2. Open-loop bandwidth of the first stage is set by local feedback, and is about 100 kHz.

This line-driver circuit has an overall gain of about 5X, as set by the R1-R2 loop. U2 is a dual current-feedback amplifier, allowing 50 mA or more of output while buffering U1.

Compensation for V1-V2 errors in U1 (a JFET-input op amp) is provided by RC, set equal to RS. With a variable RS such as a volume control, a nominal gain value is used, in this case 2-3 k Ω .

First-stage open-loop bandwidth control is exercised in this circuit, as it applies to U1 and the local feedback loop RD-RC. For the values shown, U1's open-loop bandwidth is about 100 kHz. Were RD open, the U1 stage would function as a more-conventional (narrow bandwidth) op-amp.

Control of V3-V4 errors is not integral to this amplifier, except for the local bypassing shown. Tight regulation of \pm VS will aid this, and is recommended for noise minimization.

Summary of audio op-amp series notes: The discussions above wrap up our look into various op-amp and circuit issues which help determine high audio performance. Over the years, I have found all of these techniques useful for improving audio circuits, and hope you will also.

Some parting comments: This column wraps up a two-year run of "Walt's Tools and Tips," an experience I have enjoyed immensely. I hope you have as well, and I thank all those who have contributed comments.

Over the next year (or more), I will be embarking on a major new project. Unfortunately, this will preclude the time expenditure it takes to put together the kind of material I like in this column. Therefore, I am taking a column sabbatical for a period of time. I hope to return to these pages sometime soon to continue these analog-oriented talks. Happy Holidays to all.

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Walt, it's been a real pleasure Tooling and Tipping with you. We'll miss you.-Bob Milne, Managing Editor