Use Multiplier Core For FM Stereo Multiplexed Transmission System

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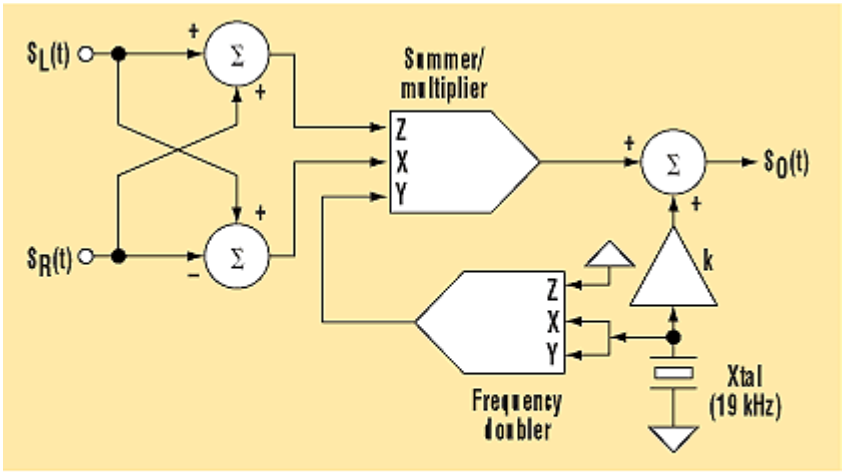
A versatile four-quadrant analog multiplier core from Analog Devices, the AD633, is widely used in applications like modulation and demodulation, automatic gain control, power measurement, and voltage-controlled amplifiers. This wide spectrum of applications is made possible by the chip's high-impedance, differential X and Y inputs, along with an accessible high-impedance summing node, Z. Designers can use the Z node to add the outputs of two or more multipliers. The output of the multiplier is given as:

W = (X2 X1)(Y2 Y1)/10 + Z

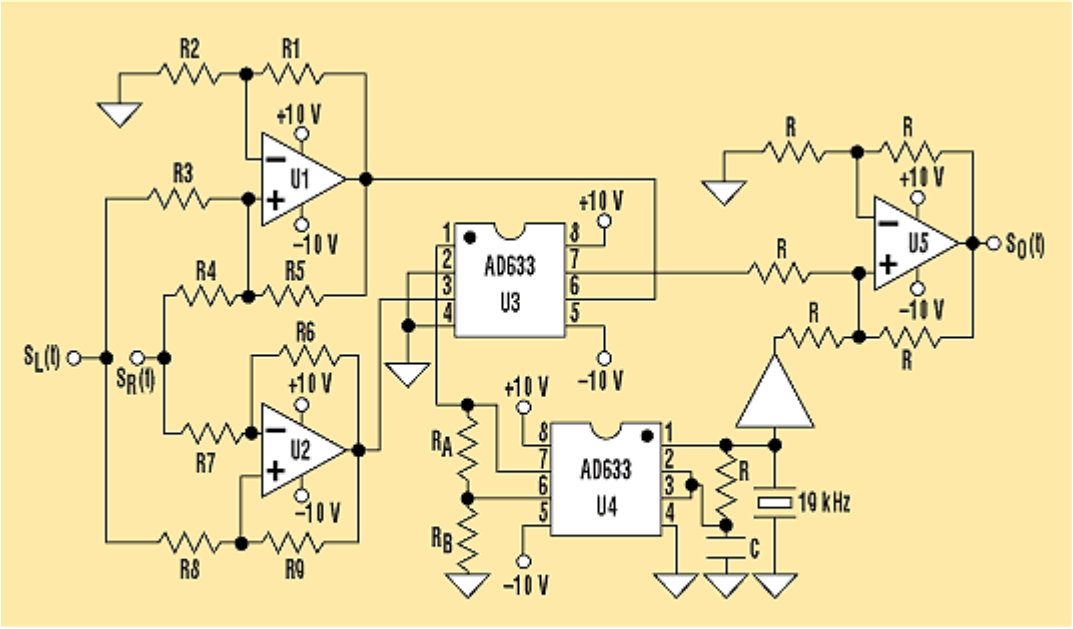
A surprisingly simple, yet robust, FM stereo multiplexed transmission system can be effectively built around this IC by using its multiplier and on-chip summer function. Figure 1 shows the basic idea for such a design. In the block diagram, SR(t) and SL(t) form the inputs from the right and left transmission microphones. These signals are applied to a matrixer that gives the sum and difference of the two inputs.



1. This block diagram illustrates the basic concept of the FM stereo multiplexed transmission system. The left (SL) and right (SR) signals are multiplexed onto a 19-kHz carrier and appear at the output (SO).

The difference signal is multiplied by a signal with twice the carrier frequency using a frequency doubler. Then, the result is added to the sum of the input signals. Note that the AD633 (U3) is effectively used as a multiplier-summer (Fig. 2). Another AD633 (U4) handles the frequency-

doubling operation. Lastly, the 19-kHz signal carrier wave is added for coherent detection.



2. The actual circuit reveals that two AD633s are used. One (U3) handles the summer/multiplier function, while the other (U4) serves as a frequency doubler.

In the design shown in Figure 2, the matrixer core is implemented by two voltage op amps, U1 and U2. Part of an LM324 quad op amp, these op amps generate the sum and difference outputs. Resistor ratios can be adjusted to fine-tune the signal strength. The difference signal is applied to U3's Y input, and the sum to the Z input. The X input is the output of the frequency doubler, U4. The RC network on frequency doubler U3 effectively eliminates the inherent dc component. Resistors RA and RB form the amplitude control. (Consult the AD633 data sheet for more information.)

For this particular implementation, the pilot carrier is selected as 19 kHz, taken from a crystal oscillator. RC values are chosen such that 1/RC approximately equals 238 kHz. Finally, the summer op-amp U5, another section of the LM324, adds the pilot carrier to the output signal appearing at pin 7 of U3. We thus have the final multiplexed signal, SO(t), that can be mathematically modeled as:

$$So(t) = C1 \cos(4pfct)[Sr(t)\ Sl(t)] + C2\ [Sl(t) + Sr(t)] + K[A\cos(2pfct)]$$

where:

$$C1 = A2/40\ \{(1 + R7/R6)[1/(1 + R7/R8)\ 1/(1 + R6/R7)]\} - 1$$

$$C2 = [(1 + R2/R1)(1/R3 + 1/R4 + 1/R5)] - 1$$

and fc and A denote the crystal frequency and amplitude level, respectively. The matrixer resistor ratio can be set to have appropriate voltage levels of the sum and difference signals.